WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

(a) a plurality of reference cells;

(b) a plurality of memory cells, data stored in a selected reference cell among said reference cells being compared to data stored in a selected memory cell among said memory cells;

(c) an address transition detector for detecting transition in input of addresses by which a memory cell is selected among said memory cells, and transmitting an address transition detecting signal indicative of the detected transition;

(d) a counter for counting said address transition detecting signals; and

(e) a reference cell decoder for selecting a reference cell among said reference cells in accordance with an output transmitted from said counter.

2. The semiconductor memory device as set forth in claim 1, further comprising a control signal generator which transmits a control signal to said counter, said control signal having a first logic level when said control signal generator receives said address transition detecting signal from said address transition detector, and a second logic level at a time at which a reference word line is to be activated.

3. The semiconductor memory device as set forth in claim 1, wherein said selected reference cell is compared to said selected memory cell for checking data when data is read out of, written into or erased out of said memory cell, and at least one reference cell is selected among said reference cells every predetermined number of times of comparison of said selected reference cell to said selected memory cell.

4. The semiconductor memory device as set forth in claim 1, wherein said plurality of reference cells is arranged for each of memory cell arrays or for a plurality of memory cell arrays.

5. The semiconductor memory device as set forth in claim 1, further comprising means for allowing said reference cells to have desired electrical property.

6. The semiconductor memory device as set forth in claim 5, wherein said electrical property includes a threshold voltage, an on-current, an off-current, an on-resistance, an off-resistance, an inverted threshold magnetic field and polarization of said reference cell.

7. The semiconductor memory device as set forth in claim 1, wherein said counter includes a plurality of stages each transmitting an output signal by which a reference cell is selected among said plurality of reference cells.

8. The semiconductor memory device as set forth in claim 1, further comprising a circuit including a metal oxide semiconductor field effect transistor (MOSFET), and wherein a current running through said circuit is checked for allowing a common current to run through said reference cells.

9. The semiconductor memory device as set forth in claim 1, further comprising a circuit including a memory device having the same threshold as that of said reference cells for adjusting threshold of said reference cells.

10. The semiconductor memory device as set forth in claim 1, wherein said semiconductor memory device is comprised of a ferroelectric memory device, and said memory cells and said reference cells are comprised of ferroelectric

capacitors and selectively controlled MOSFETs, respectively.

11. The semiconductor memory device as set forth in claim 1, wherein said semiconductor memory device includes a plurality of blocks one of which is selected in accordance with a received address signal.

12. The semiconductor memory device as set forth in claim 1, wherein said semiconductor memory device is comprised of a flash electrically erasable and programmable read only memory (EEPROM).

13. The semiconductor memory device as set forth in claim 1, wherein said semiconductor memory device is comprised of a MONOS memory.

14. The semiconductor memory device as set forth in claim 1, wherein said semiconductor memory device is comprised of a MRAM.

15. A method of selecting a reference cell among a plurality of reference cells in a semiconductor memory device including a plurality of memory cells and a plurality of reference cells, comprising:

detecting transition in input of addresses by which a memory cell is selected among said memory cells, and transmitting a pulse each time of detection;

counting said pulses; and

selecting a desired reference cell among said reference cells in accordance with the number of said pulses.